IDEC Chip Design Contest

An Adaptive Gate Driver-Assisted Continuously Scalable-Conversion-Ratio Switched-Capacitor Converter

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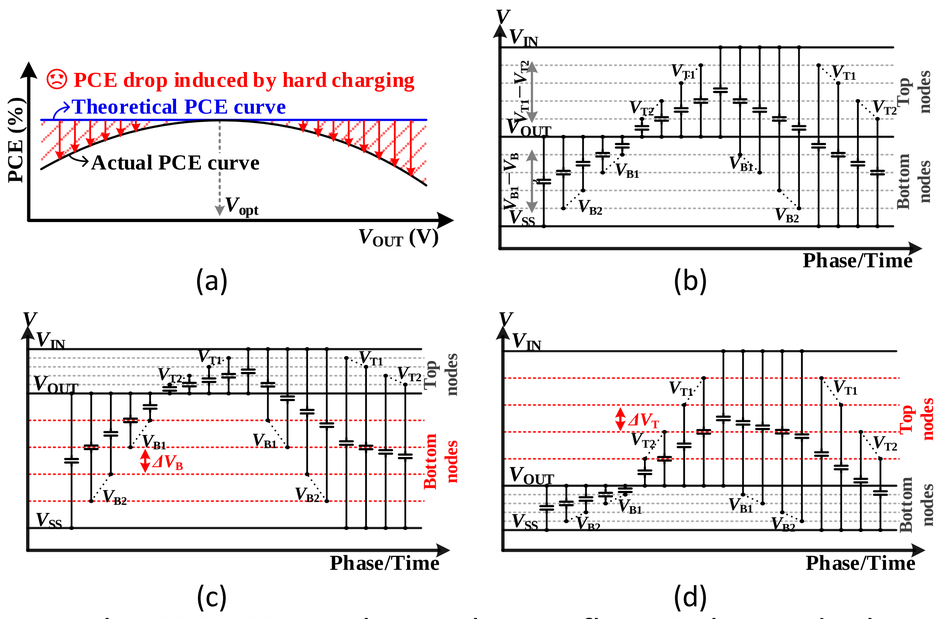
Introduction

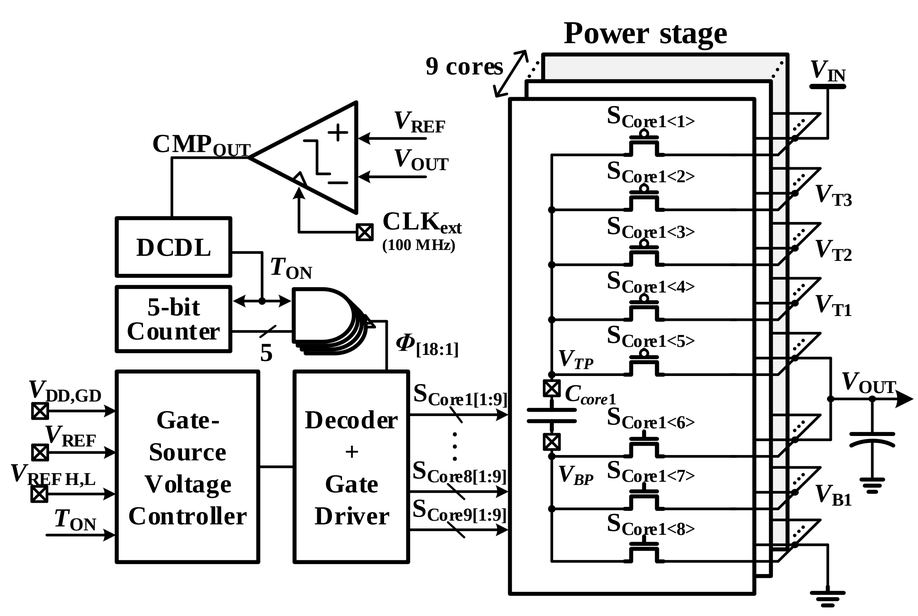
This poster presents an adaptive gate driver-assisted continuously scalable-conversion-ratio (CSCR) switched-capacitor (SC) DC-DC converter. Gate-source voltage controller (GSVC) generates dynamic supply voltage to the gate driver adaptively according to the output voltage level of the converter. By adopting an adaptive gate driver to achieve soft charging between capacitor connections, the overall system generates a wide range of output with high power density and power conversion efficiency. The proposed converter generates an output ranges from 0.7 V to 1.8 V from an input voltage of 2.9 V. The proposed converter achieves a peak PCE of 72%. The proposed converter is implemented in TSMC 180 nm BCD process, with a chip area of 3 mm x4 mm.

Design target of GSVC



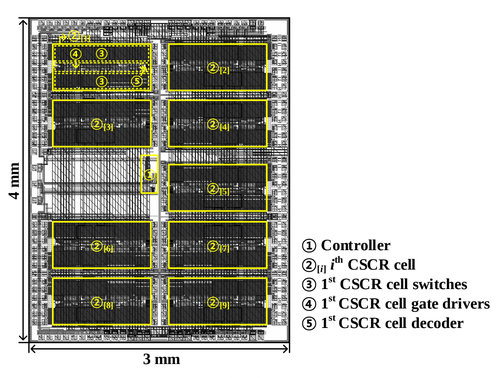
- The CSCR SC topology achieves flat PCE by gradual charge sharing, but VOUT deviation from Vopt induces hard charging loss (a).
- Regulating VOUT above V_{opt} increases ΔV_B and causes bottom-node loss (c), while regulating below V_{opt} increases ΔV_T and causes top-node loss (d).
- Precise regulation at V_{opt} is essential to maintain efficient charge sharing and maximize PCE (b).

Top block diagram

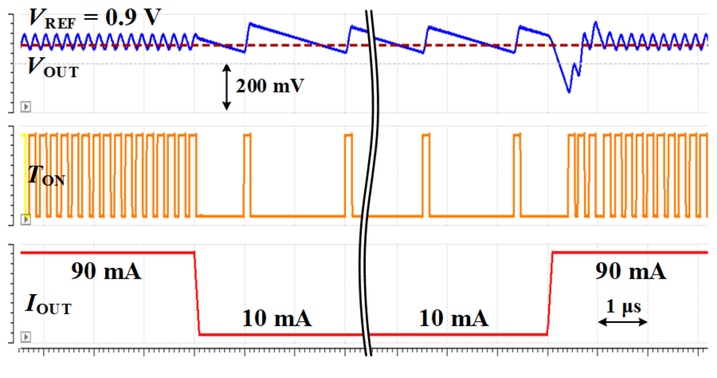


- The power stage comprises nine SC core cells, each with five switches at the top and three at the bottom of C_{core}.
- A CMP_{OUT} triggers the T_{ON} signal based on V_{OUT}–V_{REF} comparison, with the off-time controlled by the DCDL.
- The T_{ON} signal is distributed into 18 phase signals ($\Phi_{[1:18]}$) via AND gates and decoder to drive the SC cores.
- The GSVC adaptively supplies the gate drivers with V_{DD} and GND by monitoring V_{REF} against $V_{REF,H}$ and $V_{REF,L}$.

Result and Conclusion



(a)



(b)

	[1]	[2]	[3]	[4]	**This Work**
Process	65nm CMOS	180nm BCD	28nm CMOS	65nm CMOS	**180nm BCD**
V_{IN} (V)	1.5	2.5–5	2	0.4–2.5	**2.9–3**
V_{OUT} (V)	0.18–1.19	0.1–3.67	0–2.22	0.4–2	**0.7–1.8**
# of VCR	4	9	CSCR	CSCR	**CSCR**
$C_{FLY,total}$ (nF)	400 (Off-chip)	49.23 (MOS, MIM)	0.458 (MOS, MOM)	19.8 (MOS, MOM)	**300 (Off-chip)**
$I_{OUT,max}$ (mA)	400	362*	3*	19.8*	**500**
PCE_{max} [%]	93.7	87	93	90	**72**

* Estimated based on the study

(c)

- (a) shows a chip layout. The converter is implemented in a 0.18-μm BCD process, and occupies 12 mm^2 active area.
- (b) shows the simulated waveforms of the load-transient response.
- (c) shows comparison with the state-of-the-art SC converters.
- An adaptive gate driver-assisted CSCR SC converter integrates nine core cells featuring three top and one bottom flying node. The proposed GSVC modulates the V_{GS} of power switches to reduce capacitor current, transitioning C_{core} connections from hard to soft charging operation. As a result, the converter achieves a wide output voltage range beyond the non-optimal VCR range.

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

[1] Y. Jiang et al., *JSSC*, vol. 57, no. 10, pp. 2919-2933, Oct. 2022
[2] H. Kim et al., *IEEE JSSC*, vol. 59, no. 10, pp. 3444-3456, Oct. 2024
[3] N. Butzen et al., *IEEE JSSC*, vol. 54, no. 4, pp. 1039–1047, Apr. 2019.
[4] Y. Wang et al., *IEEE ISSCC* Dig. Tech. Papers, pp. 450-451Feb. 2023.